Faculty Performance Appraisal Report

Title	Dr.	First Name	Harsupreet	Last Name	Kaur	Photograph
Designation		Assistant Professor				
Address		Department of Electronic Science University of Delhi South Campus New Delhi – 110 021				
Phone No Office		011-24157199				
Residence						
Mobile		9811905600				
Email		harsupreetkaur@gmail.com				
Web-Page						

Educational Qualifications		
Degree	Institution	Year
Ph.D.	University of Delhi	2008
PG (M.Sc Physics)	University of Delhi	2003
UG (B.Sc (H) Physics	University of Delhi	2001

Career Profile

Organization	Designation	Duration	Role
Department of Electronic Science, UDSC	Assistant Professor	April 2013 till date	Teaching & Research
Bhaskaracharya College of Applied Sciences, University of Delhi	Assistant Professor	2011- April 2013 (Ad-hoc)	Teaching & Research
Deen Dayal Upadhyaya College, University of Delhi	Assistant Professor	2009-2011 (Ad-hoc)	Teaching & Research
Acharya Narendra Dev College, University of Delhi	Lecturer/ Assistant Professor	2007- 2009 (Ad-hoc)	Teaching & Research

Administrative Assignments

2018 - 2019

Member - Board of Research Studies (BRS) (Faculty of Interdisciplinary Sciences, DU)
Nodal Officer - Dept. of Electronic Science for NAAC
Election Officer - South Delhi Campus Students Union Elections 2018
Member - Undergraduate Examination Committee (For B.Sc(H) Electronics/ Instrumentation courses running in undergraduate colleges of Delhi University)
Member - Library Committee
Member - MSc Electronics Syllabus revision committee
Member – Department Research Committee
Member – Committee of Courses
Nodal officer for Foreign students for Dept. of Electronic Science
Member - Student Grievance committee

2017-2018

Member - Board of Research Studies (BRS) (Faculty of Interdisciplinary Sciences, DU)
Nodal Officer - Dept. of Electronic Science for NAAC
Election Officer - South Delhi Campus Students Union Elections 2017
Coordinator - M.Sc Electronics Entrance examination (2018)
Coordinator - M.Sc Electronics Admissions (2018)
Member - Ph.D Electronics Entrance exam committee (2018)
Member - M.Tech Microwave Electronics Entrance exam committee (2018)
Member - Undergraduate Examination Committee (For B.Tech/B.Sc(H) Electronics/ Instrumentation courses running in undergraduate colleges of Delhi University)
Member - Library Committee
Member - MSc Electronics Syllabus revision committee
Member – Department Research Committee
Member – Committee of Courses

2016-2017

Nodal Officer - Dept. of Electronic Science for NAAC
Election Officer - South Delhi Campus Students Union Elections 2016
Coordinator - M.Sc Electronics Entrance examination (2016)
Coordinator - Ph.D Electronic Science Entrance examination
Coordinator - M.Sc Electronics Admissions (2016)
Coordinator - Ph.D Electronic Science Admissions (2016)
Member - M.Tech Microwave Electronics Entrance exam committee
Member - Undergraduate Examination Committee (For B.Tech/B.Sc(H) Electronics/ Instrumentation courses running in undergraduate colleges of Delhi University)
Member - Library Committee
Member – Department Research Committee
Member – Committee of Courses

2015-2016

Nodal Officer - Dept. of Electronic Science for NAAC
Election Officer - South Delhi Campus Students Union Elections 2015
Coordinator - Annual Visitors' Program
Coordinator - M.Sc Electronics Entrance examination
Coordinator - M.Sc Electronics Admissions
Member - M.Tech Microwave Electronics Entrance exam committee
Member - Undergraduate Examination Committee (For B.Tech/B.Sc(H) Electronics/ Instrumentation courses running in undergraduate colleges of Delhi University)
Member - Library Committee
Member – Department Research Committee
Member – Committee of Courses

2014-2015

Nodal Officer - Dept. of Electronic Science for NAAC
Co-coordinator - M.Sc Entrance examination
Member - Board of Research Studies (BRS) (Faculty of Interdisciplinary Sciences, DU)
Member - Admission committee
Member - Undergraduate Examination Committee (For B.Sc(H) Electronics/ Instrumentation courses

running in undergraduate colleges of Delhi University)
Member - Library Committee
Member – Department Research Committee
Member – Committee of Courses

2013-2014
Member - Board of Research Studies (BRS) (Faculty of Interdisciplinary Sciences, DU)
Member - Departmental Research Committee
Member - Write off Committee (2013-2014)
Member - Undergraduate Examination Committee (For B.Sc(H) Electronics/ Instrumentation courses running in undergraduate colleges of Delhi University)
Member - Library Committee
Coordinator - M.Sc Admissions 2014
Member – Department Research Committee
Member – Committee of Courses

Areas of Interest / Specialization

Areas of Interest:

- **Modeling, Design and Simulation of Novel and Advanced MOSFET Structures.**
- **Modeling and Simulation of GaN MESFETs**

Specialization: Microelectronics

Subjects Taught

M.Sc Electronics
Theory Papers: Network Analysis and Synthesis, Advanced Analog Circuit Design, Electromagnetics, Analog communication, VLSI Circuit Design and Device Modeling,
Laboratory classes: Electronic Circuits, Circuit Design and simulation

Ph.D (Electronic Science)
Coordinator - Research methodology paper (2016 - till date)

Research Guidance

List against each head (If applicable)

1. *Supervision of awarded Doctoral Thesis*
2. *Supervision of Doctoral Thesis, under progress -* ***02 (02 submitted)***
3. *Supervision of awarded M.Phil dissertations*
4. *Supervision of M.Phil dissertations, under progress*
5. *Supervision of M.Sc Major projects-* ***26 (Work of some of these has resulted in the following papers in International conferences):***

    - Somishang Jagoi, Divya Pawar and Harsupreet Kaur, "Efficacy of Non-Uniformly Doped and Multi-layered Gate Dielectric Designs in Improving Device Perfomance of Elliptical MOSFETs", Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) held at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.

- Priyanka Pandey, Pooja Puri and Harsupreet Kaur, “Dual Material Gate-Gate Stack-Elliptical Gate All Around (DMG-GS-EG) MOSFET– A Novel Device Concept for Improved Performance”, International Conference on Advances in Electronics, Computers and Communications (ICAECC 2018) held at Reva University, Bangalore, India, 9th-10th February 2018.

- Monika Bansal and Harsupreet Kaur, “Analytical Threshold Voltage Model to study the impact of Graded-Channel (GC) design and gate dielectric engineering on device performance of Tri-Gate MOSFET”, presented (ORAL) in International Conference on Recent Innovations in Engineering and Technology (ICRIEAT 2016), held at Hotel Katriya, Hyderabad, India, 22nd-23rd December 2016.

- Harsupreet Kaur, Hema Mehta, "Analytical Modeling of Gate Oxide Engineered Junctionless SOI MOSFET with Vertical Gaussian-like Doping Profile", ICMARS 2014, 9-12 Dec 2014, Jodhpur, India.

Publications Profile

List against each head(If applicable) (as Illustrated with examples)

1. *Books/Monographs (Authored/Edited)*
2. *Research papers published in Refereed/Peer Reviewed Journals*
3.
   a) *Research papers published in Academic Journals other than Refereed/Peer Reviewed Journals*
   b) *Research papers published in Refereed/Peer Reviewed Conferences*
   c) *Research papers Published in Conferences/Seminar other than Refereed/Peer Reviewed Conferences*
4. *Other publications (Edited works, Book reviews, Festschrift volumes, etc.)*

RESEARCH PAPERS PUBLISHED IN REFERRED/ PEER REVIEWED JOURNALS

1. Priyanka Pandey and Harsupreet Kaur,Improved Temperature Resilience and Device Performance of Negative Capacitance Reconfigurable Field Effect Transistors, IEEE Transactions on Electron Devices,Vol. 67 No. 2.DOI:10.1109/TED.2019.2961876.

2. Monika Bansal and Harsupreet Kaur, “Device and Circuit Level Analysis of Negative Capacitance Hybrid CMOS: A Prospect for Low Power/Low Voltage Applications,” Semiconductor Science and Technology, vol. 35, no. 1, pp. 015014, Jan. 2020. DOI: 10.1088/1361-6641/ab57b4

3. Hema Mehta and Harsupreet Kaur, "Performance Assessment of Symmetric Double Gate Negative Capacitance Junctionless Transistor with High-k Spacer at Elevated Temperatures", Advances in Natural Sciences: Nanoscience and Nanotechnology Jointly Published by VAST (VN) and IOP (UK) vol. 10, no. 3, pp. 035013, Sept. 2019. DOI: 10.1088/2043- 6254/ab3d2e

4. Hema Mehta and Harsupreet Kaur , "Superior Performance and Reliability of Double Gate Gaussian Doped Negative Capacitance Junctionless Transistor for 200–500 K", IETE Technical

Review, July 2019. DOI: 10.1080/02564602.2019.1642149

5. Hema Mehta and Harsupreet Kaur, "Study on Impact of Parasitic Capacitance on Performance of Graded Channel Negative Capacitance SOI FET at High Temperature" IEEE Trans. Electron Devices, vol. 66, no 7, pp. 2904-2909, Jul. 2019. DOI: 10.1109/TED.2019.2917775

6. Hema Mehta and Harsupreet Kaur, "Subthreshold Analytical Model for Dual-Material Double Gate Ferroelectric Field Effect Transistor (DMGFeFET))" Semiconductor Science and Technology, vol. 34, pp. 065008, 2019, DOI: 10.1088/1361-6641/ab194d

7. Monika Bansal and Harsupreet Kaur. Analysis of Negative-Capacitance Germanium FinFET With the Presence of Fixed Trap Charges, IEEE Transactions on Electron Devices, 66(4), 2019, 1979 - 1984

8. Monika Bansal and Harsupreet Kaur, " An analytical subthreshold current model for ferroelectric SiGe-on-insulator field effect transistor (FSGOIFET)" Semiconductor Science and Technology, Vol.34, no.1, December 2018.

9. Hema Mehta and Harsupreet Kaur, "Impact of Gaussian Doping Profile and Negative Capacitance Effect on Double Gate Junctionless Transistors (DGJLT)" IEEE Trans. Electron Devices, , vol. 65, no. 7, pp. 2699–2706, Jul. 2018. DOI: 10.1109/TED.2018.2832843.

10. Monika Bansal and Harsupreet Kaur, "Impact of negative capacitance effect on Germanium Double Gate pFET for enhanced immunity to interface trap charges" Superlattices and Microstructures, vol. 117, pp. 189-199, 2018, DOI: 10.1016/j.spmi.2018.03.001.

11. Hema Mehta and Harsupreet Kaur, "Impact of interface layer and metal workfunction on device performance of ferroelectric junctionless cylindrical surrounding gate transistors" Superlattices and Microstructures, DOI: 10.1016/j.spmi.2017.06.032.

12. Hema Mehta and Harsupreet Kaur, "High temperature performance of Si:HfO2 based long channel Double Gate Ferroelectric Junctionless Transistors" Superlattices and Microstructures, vol. 103, pp. 78-84, 2017.

13. Hema Mehta and Harsupreet Kaur, "Modeling and simulation study of novel Double Gate Ferroelectric Junctionless (DGFJL) transistor" Superlattices and Microstructures, vol. 97, pp. 536-547, 2016

14. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Graded Channel (GC) design in fully depleted cylindrical/surrounding gate MOSFET (FD CGT/SGT) for improved short channel immunity and hot carrier reliability" Solid State Electronics, vol. 51, pp.398-404, 2007.

15. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, An analytical drain current model for graded channel cylindrical/surrounding gate MOSFET, Microelectronics Journal, vol.38, pp.352-359, 2007.

16. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "An Analytical Threshold Voltage Model for Graded Channel Asymmetric Gate Stack (GCASYMGAS) Surrounding Gate MOSFET" Solid State Electronics, vol. 52, pp.305-311, 2008.

17. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Laterally Asymmetric Channel and Gate Stack Design on Device Performance of Surrounding Gate MOSFETs : A Modeling and Simulation Study", Vol. 52, no. 3, pp. 746-750, 2010 Microwave and Optical Technology Letters

18. Sneha Kabra, Harsupreet Kaur, Ritesh Gupta, Subhasis Haldar, Mridula Gupta and R.S.Gupta "A Semi Empirical Approach for Submicron GaN MESFET Using an Accurate Velocity Field Relationship for High Power Applications", Microelectronics Journal, vol. 37, no.7, pp.620-626, 2006.

19. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta "An Analytical Model for GaN MESFET's Using New Velocity-Field Dependence" Physica Status Solidi C, vol. 3, no. 6, pp. 2350-2355, 2006.

20. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, "Two Dimensional Subthreshold Analysis of Sub-Micron GaN MESFET" Microelectronics Journal, vol. 38, no. 4-5, pp. 547–555, 2007.

21. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, "A Semi-Empirical Model for Admittance and Scattering Parameters of GaN MESFET for microwave circuit applications" Volume 49, Issue 10, October 2007, Pages: 2446-2450, Microwave and optical technology Letters.

22. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, "Temperature Dependent Analytical Model of sub-micron GaN MESFETs for Microwave frequency Applications", Vol. 52, no. 1, 25-30, 2008, Solid State Electronics.

INTERNATIONAL CONFERENCES

1 Priyanka Pandey and Harsupreet Kaur, "Performance Assessment of Polarity Tunable–Ferroelectric–Field Effect Transistor at High Temperature —Part I", IEEE 5thInternational Conference on Devices, Circuits and Systems (ICDCS -2020), Coimbatore, 5-6Mar. 2020.

2 Priyanka Pandey and Harsupreet Kaur, "Performance Assessment of Polarity Tunable–Ferroelectric–Field Effect Transistor at High Temperature —Part II", IEEE ^{5th}International Conference on Devices, Circuits and Systems (ICDCS -2020), Coimbatore, 5-6Mar. 2020.

3 Priyanka Pandey and Harsupreet Kaur,Enhanced Reliability of Polarity Controllable– Ferroelectric–FETs under the Impact of Fixed Trap Charges, Springer 3rdInternational Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 28-29Sept. 2019.

4 Priyanka Pandey and Harsupreet Kaur,Effect of SBT Ferroelectric Layer on Polarity Controllable FETs for Improved Current Drivability, IEEE 16thINDICON 2019, Gujrat, 13-15Dec. 2019.

5 Priyanka Pandey and Harsupreet Kaur,Impact of Fixed Trap Charges on the Device Performance of Polarity Controllable–Ferroelectric–Field Effect Transistor, IEEE 20th International Workshop on Physics of Semiconductor Devices(IWPSD-2019), Kolkata, 17-20Dec. 2019.

6 H. Mehta and H. Kaur, "Junctionless Gaussian Doped Negative Capacitance SOI Transistor: Investigation of Device Performance for Analog and Digital Applications," International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, Uttar Pradesh, India, 2019.

7 M. Bansal and H. Kaur, "Circuit Analysis of Pass Transistors and Inverter based on Negative Capacitance Silicon-Germanium Double Gate FET (NCSiGeDGFET)," in Proc. IEEE Global Conference for Advancement in Technology (GCAT), Bangalore, India, 18th-20th October 2019.

8 M. Bansal and H. Kaur, "Study to find the applicability of Germanium FinFET with Negative Capacitance for High Temperatures Applications", IEEE International Conference on Signal Processing, Computing and Control (ISPCC), Solan, India, 10th-12th October 2019

9 M. Bansal and H. Kaur, "Study to Analyze the Impact of Fixed Trap Charges on the Performance of Germanium Ferroelectric Double Gate FET (GeFeDGFET)," IEEE International Conference On Computing, Power and Communication Technologies (GUCON), Greater Noida, Uttar Pradesh, India,27th-28th September 2019.

10 Priyanka Pandey and Harsupreet Kaur," Surface Potential Model for Ferroelectric Nanowire Field Effect Transistor with NiSi2 Source/Drain", IEEE International Conference on Emerging Electronics (ICEE) 2018 held at Royal Orchid Resort and Convention Centre, Bangalore, India, 16th-19th December 2018.

11 Monika Bansal and Harsupreet Kaur, "Ferroelectric GeSn On Insulator FET: Device and Circuit Analysis for Steep Switching Applications", IEEE International Conference on Emerging Electronics (ICEE) 2018 held at Royal Orchid Resort and Convention Centre, Bangalore, India, 16th-19th December 2018.

12 Priyanka Pandey and Harsupreet Kaur, "Impact of SBT Ferroelectric layer on Reconfigurable FETs for Steep Switching Characteristics and Improved Performance", IEEE 4th International Conference for Convergence in Technology (I2CT), SDMIT Mangalore, 27-28 October 2018.

13 Priyanka Pandey and Harsupreet Kaur, "Drain Current Model of Reconfigurable Ferroelectric Field Effect Transistor (R-Fe-FET)", IEEE 4th International Conference for Convergence in Technology (I2CT), SDMIT Mangalore, 27-28 October 2018.

14 Somishang Jagoi, Divya Pawar and Harsupreet Kaur, "Efficacy of Non-Uniformly Doped and Multi-layered Gate Dielectric Designs in Improving Device Perfomance of Elliptical MOSFETs", Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) held at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.

15 Monika Bansal and Harsupreet Kaur, "Impact of Ferroelectric Material Properties on Device Characteristics of Ferroelectric Ge0.97Sn0.03 Double Gate FET (FEGeSnDGFET)", in IEEE International Microwave and RF Conference (IMaRC) 2018 to be held at Bharati Hotel Novotel, Kolkata, India, 28th-30th November 2018.

16 Hema Mehta and Harsupreet Kaur, "Performance Assessment of Symmetric Double Gate Negative Capacitance Junctionless Transistor with High-k Spacer at Elevated Temperatures" in NANOCON-2018 International Conference on Nanotechnology, to be held at, Bharati Vidyapeeth University, Pune, Maharahstra, from October 25-26, 2018.

17 Monika Bansal and Harsupreet Kaur, "Superior Device Performance and Reliability of Germanium Ferroelectric Double Gate FET (GeFeDGFET) at High Temperatures", in NANOCON 2018 to be held at Bharati Vidyapeeth University, Pune-Satara Road Campus, Pune, India, 25th-26th October 2018.

18 Monika Bansal and Harsupreet Kaur, "Ferroelectric-Insulator-Germanium Double Gate (F-I-GeDG) FET with steep switching characteristics and improved current drivability", in IEEE International Conference On Computing, Power And Communication Technologies 2018 (GUCON) held at Radisson Blu Hotel, Greater Noida, Uttar Pradesh, India, 28th-29th September 2018.

19 Monika Bansal and Harsupreet Kaur, "Improvement in switching characteristics of Ferroelectric-Insulator-Germanium Double Gate (F-I-GeDG) FET for ultra low power applications", in IEEE International Conference On Computing, Power And Communication Technologies 2018 (GUCON) held at Radisson Blu Hotel, Greater Noida, Uttar Pradesh, India, 28th-29th September 2018.

20 Hema Mehta and Harsupreet Kaur, "Impact of Ferroelectric HfO2 and Non-Uniform Doping on Nanoscale Planar SOI Junctionless Transistor" in GUCON-2018 IEEE International Conference on Computer, Power and Communication Technologies, held at, Radisson Blu Hotel, Greater Noida, Uttar Pradesh, from September 28-29, 2018.

21 Hema Mehta and Harsupreet Kaur, "Double Gate Graded Channel Negative Capacitance FET (DGGCNCFET): Performance Assessment for Low Power Digital/Analog Applications" in GUCON-2018 IEEE International Conference on Computer, Power and Communication Technologies, held at, Radisson Blu Hotel, Greater Noida, Uttar Pradesh, from September 28-29, 2018.

22 Monika Bansal and Harsupreet Kaur, "Negative Capacitance Germanium-Double Gate FET- A novel device concept for ultra low voltage/low power applications", in International Conference on Control, Communication and Computing 2018 (IC4) held at College Of Engineering, Trivandrum, Kerala, India, 5th-7th July 2018.

23 Monika Bansal and Harsupreet Kaur, "Performance investigation of Negative Capacitance Germanium Double Gate-pFET (NCGe-DG-pFET) for improved analog applications", presented (ORAL) in IEEE International Symposium on Devices, Circuits and Systems (ISDCS) held at IIEST, Shibpur, Kolkata, India, 29th-31st March 2018.

24 Hema Mehta and Harsupreet Kaur, "Impact of High-k spacer and Negative Capacitance on Double Gate Junctionless Transistor for Improved Short Channel Immunity and Reliability" in

ICDCS-2018 IEEE International Conference on Devices, Circuits and Systems (ICDCS'18), held at, Karunya Institute of Technology and Sciences, India, from March 16-17, 2018.

25 Hema Mehta and Harsupreet Kaur, "Performance Study of Short Channel Symmetric Double Gate Gaussian Doped Ferroelectric FET for Analog and Digital Applications" in ICDCS-2018 IEEE International Conference on Devices, Circuits and Systems (ICDCS'18), held at, Karunya Institute of Technology and Sciences, India, from March 16-17, 2018.

26 Monika Bansal and Harsupreet Kaur, " Analytical drain current model to study the impact of interface trap charges on device performance of Double Gate Ge Ferroelectric FET (DGGeFeFET)", presented (ORAL) in 3rd IEEE International Conference on Emerging Devices and Smart Systems (ICEDSS) held at Mahendra Engineering College, Namakkal DT, Tamilnadu, India, 2nd-3rd March 2018.

27 Priyanka Pandey, Pooja Puri and Harsupreet Kaur, "Dual Material Gate-Gate Stack-Elliptical Gate All Around (DMG-GS-EG) MOSFET– A Novel Device Concept for Improved Performance", International Conference on Advances in Electronics, Computers and Communications (ICAECC 2018) held at Reva University, Bangalore, India, 9th-10th February 2018.

28 Hema Mehta and Harsupreet Kaur, "Impact of Negative Capacitance Effect and Graded Channel Design on Device Performance of Double Gate MOSFET", in XIX International Workshop on The Physics of Semiconductor Devices (IWPSD 2017), held at IIT Delhi, India, from December 11-15, 2017.

29 Hema Mehta and Harsupreet Kaur, "Temperature Dependent Analytical Model for Cylindrical Surrounding Gate Ferroelectric Junctionless Transistor (CSGFJL)", in XIX International Workshop on The Physics of Semiconductor Devices (IWPSD 2017), held at IIT Delhi, India, from December 11-15, 2017.

30 Hema Mehta and Harsupreet Kaur, "Double Gate Gaussian Doped Negative Capacitance FET (DGGDNCFET): A Novel Concept for Enhanced Device Performance in INDICON-2017 14TH IEEE India Council International Conference 2017, held at, IIT Roorkee, India, from December 15-17, 2017.

31 Hema Mehta and Harsupreet Kaur, "Design Space Optimization for Nanoscale Graded Channel Negative Capacitance (GCNC) SOI MOSFET for Improved Device Performance and Temperature Resilience", in NANOfIM 2017 (Nanotechnology for Instrumentation and Measurement Workshop), held at Gautam Buddha University, Greater Noida, Uttar Pradesh, India, from November 16-17, 2017.

32 Monika Bansal and Harsupreet Kaur, "An analytical model for long channel Double Gate Ge Ferroelectric FET (DGGeFeFET) to study the impact of interface trap charges", presented (ORAL) in IEEE International Conference on Smart Technologies for Smart Nation (SmartTechCon 2017) held at Reva University, Bangalore, India, 17th-19th August 2017. Print ISSN: 978-1-5386-0570-7, Online ISSN: 978-1-5386-0569-1

33 Hema Mehta and Harsupreet Kaur, "Analytical Model to Study the Impact of Ferroelectric Materials SBT/PZT on Elliptical Gate All Around Junctionless Transistor", in IEEE TENSYMP 2017 – "Technologies for Smart Cities" to be held at Cochin, Kerala, India, from 14th-16th July, 2017.
"Technologies for Smart Cities" to be held at Cochin, Kerala, India, from 14th-16th July, 2017.

34 Hema Mehta and Harsupreet Kaur, "High Temperature Performance Investigation of Elliptical Gate Ferroelectric Junctionless Transistor", presented (ORAL) in 3rd International Conference on Emerging Electronics (ICEE) 2016, held at IIT Bombay, Mumbai, India, 27th-30th December, 2016.

35 Monika Bansal and Harsupreet Kaur, "Analytical Threshold Voltage Model to study the impact of Graded-Channel (GC) design and gate dielectric engineering on device performance of Tri-Gate MOSFET", presented (ORAL) in International Conference on Recent Innovations in Engineering and Technology (ICRIEAT 2016), held at Hotel Katriya, Hyderabad, India, 22nd-23rd December 2016.

36 Hema Mehta and Harsupreet Kaur, "Analytical Model to Study Temperature Dependent Negative Capacitance Effect on Long Channel Double Gate Ferroelectric Junctionless Transistor", presented (POSTER) in Asia Pacific Microwave Conference (APMC) 2016, held at Hotel Pullman, Aerocity, New Delhi, India, 5th-9th December, 2016.

37 Hema Mehta and Harsupreet Kaur, "Analytical Drain Current Model to Study the Impact of Negative Capacitance Phenomenon in Symmetric Double Gate Junctionless Transistor", presented (ORAL) in IEEE TENCON 2016 — Technologies for Smart Nation held at Marina Bay Sands, Singapore, 22nd-25th November, 2016.

38 Hema Mehta and Harsupreet Kaur, "Impact of Negative Capacitance phenomenon of Ferroelectric Materials SBT and PZT on Elliptical Gate All Around Junctionless Transistor", presented (POSTER) in International Conference on Advances in Nanomaterials and Nanotechnology (ICANN) 2016, held at Jamia Millia Islamia, New Delhi, I4th-5th November, 2016.

39 Hema Mehta, Harsupreet Kaur, "Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius.

40 Harsupreet Kaur, Hema Mehta, Analytical Modeling of Gate Oxide Engineered Junctionless SOI MOSFET with Vertical Gaussian-like Doping Profile, ICMARS 2014, 9-12 Dec 2014, Jodhpur, India.

41 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Laterally Asymmetric Channel and Gate Stack Design on Device Performance of Surrounding Gate MOSFETs: A Modeling and Simulation Study", Asia Pacific Microwave Conference, APMC 2008,16th -18th December 2008, Hong Kong.

42 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R.S.Gupta, "Asymmetric Multilayered Gate Dielectric (AMGAD) Surrounding gate MOSFET: A New Structural Concept for Improved Device Performance" Microwaves 2008, Jaipur, India.

43 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "A Comparative Analysis Using Modeling and Simulation to Study the Impact of Multilayered Gate Dielectric (MGD) Design on Device Performance of Surrounding Gate MOSFET", The XXIX General Assembly of the International Union of Radio Science (Union Radio Scientifique Internationale) URSI-2008, 9th - 16th August 2008, Chicago, Illinois, USA.

44 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, "Impact of Non-Uniformly Doped and Multilayered Asymmetric Gate Stack Design on Device Characteristics of Surrounding

Gate MOSFETs", Workshop on Compact Modeling (WCM-2008), 1st -5th June, Boston, Massachusetts, U.S.A.

45 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Modeling and Simulation of Graded Channel Asymmetric Gate Stack (GCASYMGAS) Surrounding Gate MOSFET", Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed mode Applications, pp.43-44, 5th -6th January, 2008, New Delhi, India.

46 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Impact of Gate Stack Architecture on Device Characteristics of Surrounding Gate MOSFETs", Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed mode Applications, pp.45-46, 5th -6th January, 2008, New Delhi, India.

47 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Impact of Laterally Asymmetric Channel and Gate Stack Architecture on Device Performance of Surrounding Gate MOSFET (LACGAS SGT): A Simulation Study", International Semiconductor Device Research Symposium (ISDRS) 2007, pp.1892-1893, 12th -14th December, 2007, University of Maryland, USA

48 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "An Analytical Model for Graded Channel Asymmetric Gate Stack Surrounding Gate MOSFET (GCASYMGAS SGT)", International Symposium on Microwave and Optical Technology (ISMOT) 2007, pp.817-820, 17th -21st December, Monte Porzio Catone, Italy.

49 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An analytical 2-Dimensional subthreshold model for drain induced barrier lowering (DIBL) effect in GaN MESFET", International Symposium on Microwave and Optical Technology (ISMOT) 2007, 17th -21st December, Monte Porzio Catone, Italy.

50 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "A Two-Dimensional Analytical Model for I-V Characteristics of Graded Channel Surrounding Gate (GC SGT) MOSFET", International workshop on physics of semiconductor devices (IWPSD) 2007, pp.236-239, 16th -18th December, Mumbai, India.

51 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Laterally Asymmetric Channel Gate Stack (LACGAS) SGT: A New Structural Concept for Improved Device Performance" International workshop on physics of semiconductor devices (IWPSD) 2007, pp.191-193, 16th -18th December, Mumbai, India.

52 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An Analytical Model for Admittance Parameters of GaN MESFET for microwave circuit applications" International workshop on physics of semiconductor devices (IWPSD) 2007, 16th -18th December, Mumbai, India

53 Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Asymmetric Gate Stack Surrounding gate Transistor (ASYMGAS SGT): 2-D Analytical Threshold Voltage Model", Asia Pacific Microwave Conference (APMC 2007), pp. 2511-2514, 11th -14th December, Bangkok, Thailand.

54 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An analytical model for high temperature operation of GaN MESFETs" CODEC 2006, 18th -20th December,

Kolkata, India.

55 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, "An Analytical Threshold Voltage Model for Sub-Micron GaN MESFET" European Workshop on III Nitride Materials and Devices 2006, 18th-20th September, Crete, Greece.

56 Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar and R.S.Gupta, "An Analytical 2-Dimensional Model for Graded Channel Fully Depleted Cylindrical/ Surrounding Gate SOI MOSFETs", International workshop on physics of semiconductor devices (IWPSD 2005), Vol.II, pp.1150-1155, 13th -17th December, New Delhi, India.

57 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta "An Analytical Model of Sub-micron GaN MESFET's using Exact Velocity Field Dependence for Microwave Applications" IWPSD'2005, 13th -17th December, New Delhi, India

58 Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar and R.S.Gupta, "Modeling and Analysis of graded channel fully depleted cylindrical/ surrounding gate SOI MOSFETs", URSI 2005, 23rd -29th October, New Delhi, India.

59 Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta "An Analytical Model for GaN MESFET's Using New Velocity-Field Dependence" International Conference on Nitride Semiconductors, ICNS'2005, 28th August-2nd September, Breman, Germany.

NATIONAL CONFERENCES

1. Hema Mehta and Harsupreet Kaur , "Theoretical Study of Impact of Ferroelectric Properties of SBT/PZT and Interface Layer on Double Gate Symmetric Junctionless Transistor", 2nd National Conference on Recent Developments in Electronics (NCRDE 2017), 17th-18th February 2017, Department of Electronic Science, University of Delhi South Campus, Delhi, India.

2. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "A Two-Dimensional Threshold Voltage Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate MOSFETs" MATEIT 2006, pp.259-262, 22nd -25th March, New Delhi, India.

3. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R.S.Gupta, "An Analytical Drain Current Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate MOSFET" Microwaves 2006, pp.116-118, 6th -8th October, Jaipur, India

4. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "Graded Channel (GC) Design in Surrounding Gate MOSFET (SGT) for Improving Short Channel and Hot Carrier Performance", Indian Microelectronics Society (IMS) 2007, pp.216-220,16th -17th August, Chandigarh, India

5. Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, "A Two-Dimensional Threshold Voltage Model for Asymmetric Gate Stack Surrounding Gate MOSFET", authored by Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta" MATEIT'2008, 26th -28th September, New Delhi, India.

6. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta, R.S.Gupta, An empirical Model for the Effective Velocity Field Characteristics in GaN MESFET Including Near Ballistic Transport and its Applications" MATEIT'2006, 22nd -25th March, New Delhi, India.

7. Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S.Gupta, “An Analytical Two Dimensional Threshold Voltage Model for Sub-Micron GaN MESFET” Microwaves’2006, 6th -8th October, Jaipur, India.

Invited Lecture delivered/Session Chair:

1 Invited talk on "Emerging Nanoelectronic Devices" at Bhaskaracharya College of Applied Sciences, University of Delhi, on 20th February, 2019

2 Session Chair - Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) organised at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.

3 Invited talk on “CMOS and VLSI Technology” at Hansraj College, University of Delhi, September 26, 2017.

4 Session Chair - International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2016) organised at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 22-23 September 2016.

5 Delivered following Invited talks at TEQIP-II Sponsored Faculty Development Programme on "Advances in Microelectronics and Plasma Diagnostics" (AMPD-2016), organized by Dept of Applied Physics, Delhi Technological University, August 29- September 2, 2016.

(i) "CMOS Scaling : Review and Perspectives"

(ii) "Material and Device Architecture Innovations for Advanced CMOS Technology"

Conference Organization/ Presentations **(last 5 years)**

List against each head(If applicable)

1. *Organization of a Conference*
2. *Participation as Paper/Poster Presenter - (last 5 years)*

1. Presented a paper, " Effect of SBT Ferroelectric Layer on Polarity Controllable FETs for Improved Current Drivability", authored by Priyanka Pandey and Harsupreet Kaur IEEE 16thINDICON 2019, Gujrat, 13-15Dec. 2019. (ORAL)

2. Presented a paper, "Enhanced Reliability of Polarity Controllable–Ferroelectric–FETs under the Impact of Fixed Trap Charges" authored by Priyanka Pandey and Harsupreet Kaur , Springer 3rdInternational Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 28-29Sept. 2019. (ORAL)

3. Presented a paper, "Efficacy of Non-Uniformly Doped and Multi-layered Gate Dielectric Designs in Improving Device Perfomance of Elliptical MOSFETs" authored by Somishang Jagoi, Divya Pawar and Harsupreet Kaur, Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) held at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018 (ORAL).

4. Presented a paper, "Design Space Optimization for Nanoscale Graded Channel Negative Capacitance (GCNC) SOI MOSFET for Improved Device Performance and Temperature Resilience", authored by Hema Mehta and Harsupreet Kaur in NANOfIM 2017 (Nanotechnology for Instrumentation and Measurement Workshop), held at Gautam Buddha University, Greater Noida, Uttar Pradesh, India, from November 16-17, 2017.(ORAL)

5. Presented a paper, "Hema Mehta and Harsupreet Kaur, "Analytical Model to Study the Impact of Ferroelectric Materials SBT/PZT on Elliptical Gate All Around Junctionless Transistor", presented in IEEE TENSYMP 2017 – "Technologies for Smart Cities", held at Cochin, Kerala, India, 14th-16th July, 2017(Oral presentation)

6. Presented a paper, "Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", authored by Hema Mehta and Harsupreet Kaur, IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius. (Oral presentation)

ORGANIZATION OF A CONFERENCE

1. Member - Abstract Registration Committee- International Conference on Renewable Energy & Emerging Technologies, 13-14 November, 2019.

2. Member – Organizing Committee - Second national Conference on Recent Developments in Electronics (NCRDE-2017) held during 17-18 February 2017, at South Campus, Delhi University.

3. . Member - Technical Program Committee - International Conference on Advances in Computers, Communication and Electronic Engineering (COMMUNE 2015) held at University of Kashmir, Srinagar during 16-18 march 2015.

4. Member – Organizing Committee: National conference on E-waste sustainability : needs and

solutions for its management" held at Bhaskaracharya College of Applied Sciences, University of Delhi during March 7-8, 2013.

Research Projects (Major Grants/Research Collaboration)

1. DU R&D project titled, " Performance Evaluation of Elliptical Gate MOSFETs Using Analytical Modeling and Simulation" 2015-2016 (Rs. 2,70,000)

2. 1. DU R&D project titled, " Modeling, Design and Simulation of Negative Capacitance Junctionless (NCJL) MOSFETs for ultra low power applications " 2014-2015 (Rs. 1,70,000)

Awards and Distinctions

- *Best paper award* - Priyanka Pandey and Harsupreet Kaur, "Performance Assessment of Polarity Tunable– Ferroelectric–Field Effect Transistor at High Temperature —Part I", IEEE 5thInternational Conference on Devices, Circuits and Systems (ICDCS -2020), held in Coimbatore, 5-6March, 2020.

- Name appeared in Golden List of Reviewers for 2019 - IEEE TRANSACTIONS ON ELECTRON DEVICES

- *Best paper award* - Monika Bansal and Harsupreet Kaur, "Study to Analyze the Impact of Fixed Trap Charges on the Performance of Germanium Ferroelectric Double Gate FET (GeFeDGFET)," IEEE International Conference On Computing, Power and Communication Technologies (GUCON), Greater Noida, Uttar Pradesh, India, 27th-28th September 2019.

- *Best paper award* - Monika Bansal and Harsupreet Kaur, "Superior Device Performance and Reliability of Germanium Ferroelectric Double Gate FET (GeFeDGFET) at High Temperatures", in NANOCON 2018 held at Bharati Vidyapeeth University, Pune-Satara Road Campus, Pune, India, 25th-26th October 2018.

- *Best paper award* - Hema Mehta and Harsupreet Kaur, "Theoretical Study of Impact of Ferroelectric Properties of SBT/PZT and Interface Layer on Double Gate Symmetric Junctionless Transistor", 2nd National Conference on Recent Developments in Electronics (NCRDE 2017), 17th-18th February 2017, Department of Electronic Science, University of Delhi South Campus, Delhi, India.

- Name listed in the *2010 edition of Who's Who in the World*

- Won the 'Young Scientist Award' in The XXIX General Assembly of the International Union of Radio Science (Union Radio-Scientifique Internationale) URSI-GA 2008 conference held in Chicago, Illinois, USA during August 7-16, 2008.

- Qualified CSIR-UGC NET and secured 7th rank in India.

- Recipient of the Delhi Sanskrit Academy Award in the Secondary Board Examination, 1996.

Association With Professional Bodies

1. *Editing - Nil*
2. *Reviewing -*

- IEEE Transactions on Electron Devices
- IEEE Journal of the Electron Devices Society
- Silicon (Springer Nature)
- International Journal of Electronics and Communications
- AIP Advances
- Japanese Journal of Applied Physics
- Journal of Electronic Materials
- International Journal of Numerical Modelling: Electronic Networks, Devices and Fields
- International Journal of Modelling and Simulation
- Optik – International Journal for Light and Electron Optics
- Journal of Electrical Engineering & Technology
- International Journal of Modelling and Simulation
- Reviewer - SERB DST proposals
- Reviewer for project proposals submitted to Executive board of Austrian Science Fund
- Reviewer - 7th International Conference on Microelectronics, Circuits and Systems, to be held during 5th-6th June, 2020 at Delhi Technological University, India.
- Member – Abstract Committee – International Conference on Renewable Energy & Emerging Technologies, November 13, 2019, Jakarta, Indonesia
- Member - Technical Program Committee - International Conference on Advances in Computers, Communication and Electronic Engineering **(COMMUNE 2015)** held at University of Kashmir, Srinagar during 16-18 march 2015.
- Reviewer for international conference**, IEEE TENCON 2016** held during 22 - 25 November 2016, Marina Bay Sands**,** Singapore.
- Reviewer for international conference**, IEEE NANOCON 2018** held during 25- 26 October 2018, Pune.

3. *Advisory*
4. *Committees and Boards*
5. *Memberships*

- Senior Member, IEEE USA (June 2018 -)
- Member, IEEE USA
- Member, Electronic Devices Society, USA
- Member -IEEE Solid-State Circuits Society
- Life Member - Semiconductor Society of India

6. *Office Bearer-*
    - Executive Member - IEEE-EDS Delhi Chapter (2013- till Dec2015)
    - Executive Member - IEEE-EDS Delhi Chapter (Jan 2019- till date)
    - Secretary - IEEE EDS Delhi Chapter (Jan 2020 -)

Other Activities

Conferences/ Workshops Attended:

1. Attended IEEE 16th INDICON 2019, Gujrat, 13-15Dec. 2019.

2. Attended Springer 3rd International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 28-29 Sept. 2019.

3. Attended Second IEEE International Conference on Microelectronics and Telecommunication Engineering 2016 (ICMETE-2018) organised at SRM University, Delhi-NCR Campus, Modinagar, Ghaziabad during 20-21 September 2018.

4. Attended Orientation Programme at Centre for professional Development in Higher Education, University of Delhi during June 08, 2018 - July 06, 2018.

5. Attended tutorial course on "III-N based RF devices" on December 11, 2017 in XIX International Workshop on the Physics of Semiconductor Devices (IWPSD 2017) organized by Solid State Physics Laboratory, Delhi and Indian Institute of Technology, New Delhi, December 11-15, 2017.

6. Attended XIX International Workshop on the Physics of Semiconductor Devices (IWPSD 2017) organized by Solid State Physics Laboratory, Delhi and Indian Institute of Technology, New Delhi, December 11-15, 2017.

7. Presented a paper, "Design Space Optimization for Nanoscale Graded Channel Negative Capacitance (GCNC) SOI MOSFET for Improved Device Performance and Temperature Resilience", authored by Hema Mehta and Harsupreet Kaur in NANOfIM 2017 (Nanotechnology for Instrumentation and Measurement Workshop), held at Gautam Buddha University, Greater Noida, Uttar Pradesh, India, from November 16-17, 2017.(ORAL)

8. Presented a paper, ""Analytical Model to Study the Impact of Ferroelectric Materials SBT/PZT on Elliptical Gate All Around Junctionless Transistor", (ORAL) in IEEE TENSYMP 2017 – "Technologies for Smart Cities", held at Cochin, Kerala, India, 14th-16th July, 2017

9. Presented a paper, "Hema Mehta and Harsupreet Kaur, Modeling and Analysis of Double Gate Ferroelectric Junctionless (DGFJL) Transistor", IEEE Radio and Antenna Days of the Indian Ocean (RADIO) 2015, 21-24 September 2015, Mauritius.

10. International Mini Workshop on VLSI systems, Jawaharlal Nehru University, New Delhi, Jan12th -13th, 2015

11. Attended a two day Mini-Colloquia from 14-15 March, 2012 held at South Campus, Delhi University.

12. Attended the Workshop on "Experiments and Research Applications with National Instruments LabVIEW" held at Bhaskaracharya College of Applied Sciences, University of Delhi during 2nd – 3rd February, 2012.

13. Attended the Workshop on "Training on ExpEYES Design Kit" held at Bhaskaracharya

College of Applied Sciences, University of Delhi on 28th January, 2012.

14. Attended the National Workshop On Recent Trends in Semiconductor Devices and Technology, Jointly Organized By FiDAS, Deen Dayal Upadhyaya College, University of Delhi And IEEE EDS Delhi Chapter, New Delhi, Supported By DRDO, Govt of India and Integrated Microsystem, Gurgaon, India held during September 17-18, 2010.

15. Attended the National Workshop On Quantum Mechanics: Theory and Application Organized By FiDAS, Deen Dayal Upadhyaya College, University of Delhi, Sponsored By CSIR, Govt of India Supported By IEEE EDS Delhi Chapter, New Delhi and The National Academy of Sciences, India, - Delhi Chapter held during October 22-23, 2010 and October 29-30, 2010.

16. Attended the National Workshop on Recent Trends in Semiconductor Devices and Technology, Sponsored By Integrated Microsystem, India, and Society for Microelectronics and VLSI, New Delhi, February 12-13, 2010 held at Deen Dayal Upadhyaya College, University of Delhi, New Delhi.

17. Attended the "!8th WIMNACT-MQ3-New Delhi, India- Workshop and IEEE EDS Mini Colloquim on Nanometer CMOS Technology, Mini Colloquia on Compact Modeling and Fabrication Techniques of Advance MOSFET/ HEMT Structures" held at University of Delhi South Campus during June 04-05, 2009 organized by IEEE EDS-Delhi Chapter, Department of Electronics Science, University of Delhi South Campus, New Delhi, India.

18. Attended a Multi-Media Workshop "Easy Now" held at Acharya Narendra Dev College, University of Delhi, New Delhi, 20 – 25 April 2009.

19. Attended the URSI-GA Conference "International Union of Radio Science" held on 7th - 16th December, 2008 at Hyatt Regency, Chicago, Illinois, USA and presented paper entitled "A Comparative Analysis Using Modeling and Simulation to Study the Impact of Multilayered Gate Dielectric (MGD) Design on Device Performance of Surrounding Gate MOSFET".

20. Attended the "Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed mode Applications" held at University of Delhi South Campus, New Delhi, India sponsored by the IEEE Electron Device Society under its Distinguished Lecturer Program, 5-6 January 2008 and presented papers entitled "Impact of Gate Stack Architecture on Device Characteristics of Surrounding Gate MOSFETs" and "Modeling and Simulation of Graded Channel Asymmetric Gate Stack (GCASYMGAS) Surrounding Gate MOSFET".

21. Attended the National Conference on Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2008)" held on 26th-28th September, 2008 at Deen Dayal Upadhyaya College, University of Delhi and presented a paper entitled "A Two-Dimensional Threshold Voltage Model for Asymmetric Gate Stack Surrounding Gate MOSFET".

22. Attended "Wiki-Ed 08" held at Acharya Narendra Dev College, University of Delhi, New Delhi between 3rd, 4th and 6th October 2008.

23. Attended a Workshop on Linux and Open System Software held at Acharya Narendra Dev College, University of Delhi, New Delhi, 6th-7th December 2007.

24. Attended the National Conference on Recent Advancements in Microwave Technique and Applications (Microwave-2006) held on 6th-8th October, 2006 at Jaipur and presented a paper entitled "An Analytical Drain Current Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate MOSFET".

25. Attended the National Conference on Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2006)" held on 24th-26th March, 2006 at Deen Dayal Upadhyaya College, University of Delhi and presented a paper entitled "A Two-Dimensional Threshold Voltage Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate MOSFETs".

26. Attended the "International Workshop on Physics of Semiconductor Devices (IWPSD) 2005"held on 13th-17th December at National Physical Laboratory, New Delhi, India and presented a paper entitled "An Analytical 2-Dimensional Model for Graded Channel Fully Depleted Cylindrical/ Surrounding Gate SOI MOSFETs".

27. Attended the URSI GA 2005 Conference "International Union of Radio Science" held between 22nd -29th October, 2005 at Vigyan Bhawan, New Delhi, India and presented a paper entitled "Modeling and Analysis of graded channel fully depleted cylindrical/ surrounding gate SOI MOSFETs".

28. Attended a short course on "Spice Models for Advanced VLSI Circuit Simulation (SMAVCS)" organized by Department of Electronic Science, University of Delhi South Campus, New Delhi, India form 11th-12th December, 2005.

Conferences/ Workshops/ Lectures Organized:

1. Joint Secretary - International Symposium on Microwave and Optical Technology (ISMOT 2020) to be held during December 19-21, 2020 at New Delhi, India.

2. IEEE-EDS Technical Lecturer Talk by Professor Cher Ming Tan, Chang Gung University, Taiwan on "Computational Reliability – A paradigm shift in product reliability assurance" at University of Delhi South Campus, New Delhi on January 28, 2020.

3. Coordinator – "Workshop on VLSI Current Trends Using Mentor Graphics & Xilinx" jointly organized by Department of Electronic Science University of Delhi South Campus and CoreEL TECHNOLOGIES (Technically sponsored by IEEE EDS Delhi Chapter) on 21-22 March, 2018 at University of Delhi South Campus.

4. Coordinator – Visitors' Program organized by Department of Electronic Science, University of Delhi South Campus, sponsored by IEEE EDS Delhi Chapter and IEEE MTT-S Student Branch Chapter, IIT Delhi on March 12, 2016 at University of Delhi South Campus.

5. IEEE-EDS Technical Lecturer Talk by Dr. Amitava Sen Gupta, Scientist- H, Time and frequency standards department, National Physical Laboratory on "Atomic Clocks- How do they work and why do we need them?" at University of Delhi South Campus, New Delhi on November 14, 2014.

6. Member – Organizing Committee: Workshop on "Training on ExpEYES Design Kit" held at Bhaskaracharya College of Applied Sciences, University of Delhi on 28th January, 2012.

7. Member – Organizing Committee: The 12th International Symposium on Microwave and Optical Technology (ISMOT- 2009) held at Hotel Ashok, New Delhi, India from 16-19, December 2009.

8. Member- Organizing Committee: The 18th *WIMNACT(Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology)-New Delhi, India* - Mini-Colloquia on "Compact Modeling and Fabrication techniques of advance MOSFET/ HEMT structures", June 04-05, 2009 at University of Delhi South Campus, New Delhi, India sponsored by the IEEE Electron Device Society under its Distinguished Lecturer Program.

9. Member – Local Organizing Committee, 16th Asia-Pacific Microwave Conference (APMC'2004), held during Dec'15-18 2004, New Delhi, India.

Other Information:

1. Resource person & Judge in interdisciplinary workshop "New Frontiers in Science" organized by Acharya Narendra Dev College on 22 October 2019 at 09.00 am.

2. Judged the Hardware projects organized for students of Delhi-NCR by Project WIE Stand, IEEE WIE Delhi Section on 29 April 2017 at University of Delhi, South Campus.

3. Member - TIC CLUB, Electropreneur Park, University of Delhi South Campus (2016-2017)

4. Mentored a student, Sundaram Yadav, student of B.Tech (Electronics) of Acharya Narendra Dev College for the Summer Internship Programme in Laboratory Research organized by CIC-Centre for Science Education and Communication during June - July 2016.